Nickel Nanodots for Memory Devices

Anthony J. Pacifico

***Abstract*—The formation of Nickel Nanodots (Ni-ND) were studied for the purpose of their potential use in memory devices. Ni-NDs were formed on SiO_2 and integrated into capacitors. These structures were then tested to demonstrate charge storage characteristics.**

***Index Terms*—Floating-Gate Memory, Nickel Nanodots, Trapped Oxide Charge**

I. INTRODUCTION

FUTURE scaling of technologies demand innovation and optimization of current technologies. In semiconductor chip manufacturing, as the device features shrink, process parameters and designs must be modified to account for this. These process or design changes can lead to challenges with reliability, yield and performance, thus the on-going quest for new and innovative processes. Among these technologies which may undergo redesign or replacement is that of floating-gate memory devices. As the dimensions of these devices shrink, dielectric film thicknesses must be adjusted or replaced with different k dielectrics to ensure proper functionality. However with decreasing oxide thicknesses, the devices are more prone to leakage. Additionally the replacement of SiO_2 with other dielectrics reduces the performance of the devices. Electrically isolated Ni-NDs would provide a possible alternative to current floating-gate memory. This could reduce the potential for total device failure without the reduction of performance due to the introduction of different dielectrics.

II. THEORY

The formation of nickel nanodots (Ni-NDs) is the result of several mechanisms. The first mechanism is that of thermal evaporation of a nickel (Ni) film. The second mechanism of their formation is the result of self-agglomeration due to the surface diffusion of Ni. The combination of these two mechanisms and their interactions with each other is the focus of this work and how the Ni-NDs were formed.

The importance of Ni-NDs lies in their ability to be used as charge storage sites. These charge storage sites will act similar to that of a traditional non-volatile floating-gate memory. Floating-gate memory functions on the ability to program a device by charging it or de-charging it and the devices response to the programming. First to understand this concept, the basic Metal-Oxide-Semiconductor (MOS) charge-voltage (C-V) characteristics must be understood.

One parameter which maintains a significant role in determining the characteristics of a MOS device is that of the threshold voltage (V_T). The V_T is commonly referred to as the "turn-on" voltage, or the voltage at the onset of inversion in-which current begins conducting. This parameter is a function of many factors, but for the purpose of this work the interest is focused on the oxide charge which alters the V_T.

Several factors typically treated as non-idealities or defects in terms of MOS transistors (MOSFETS) alter a flat-band voltage (V_{FB}). This V_{FB} is the main interest of this work and how it affects the characteristics of MOS device. The V_{FB} is the condition in which there is zero band bending or no electric field in the semiconductor. This marks the dividing line between accumulation and depletion. The following equation 1 illustrates the calculation of V_{FB} [1].

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M}{C_O} - \frac{Q_{IT}}{C_O} \quad (1)$$

Where ϕ_{MS} is the gate metal workfunction, $\frac{Q_F}{C_O}$ is the fixed oxide charge, $\frac{Q_M}{C_O}$ is the mobile ionic charge and $\frac{Q_{IT}}{C_O}$ is the interfacial trapped charge. These non-idealities can be used to understand how Ni-NDs would affect the C-V characteristics of a MOS device. As Ni-NDs would essentially act in a similar mannerism as they store charge in the oxide. These non-idealities however, are unwanted and not a result of design. The following equation 2 illustrates the basic relationship between V_T and V_{FB}.

$$V_T = V_{T,} + V_{FB} \quad (2)$$

Where V_T is the actual threshold voltage of the device and $V_{T'}$ is the ideal case without non-idealities. In terms of C-V characteristics of a MOS device, there exist two separate tests which can be performed. C-V sweeps are performed by sweeping a d.c. voltage with a superimposed small a.c. signal on top. A low frequency C-V sweep can be performed to give d.c. like characteristics where minority carriers have sufficient time to generate and recombine. A high frequency sweep (~1MHz) however doesn't allow the recombination-generation

This work was presented at the 27th Annual Microelectronic Engineering Conference on May 12, 2009 at the Rochester Institute of Technology (RIT). This study was conducted to fulfill the senior design project requirement for the B.S. degree in Microelectronic Engineering.

A. J. Pacifico is with the Rochester Institute of Technology, Rochester, NY 14623 USA (phone: 716-982-8860; e-mail: ajp6155@rit.edu).

process to supply or eliminate the minority carriers as a result of the a.c signal. Thus fixing the number of minority carriers at its d.c. value. The following figure 1 illustrates the typical behavior[2] of a p-type MOS structure.

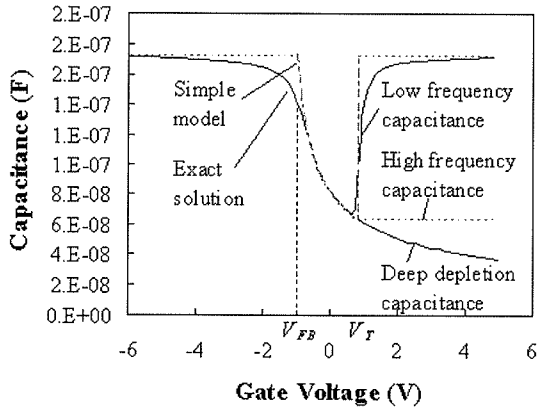

Fig. 1. Typical C-V characteristics of a p-type MOS device [2]

The focus of this work is using a designed shift in the V_{FB} as measured via C-V sweeps of a MOS device to demonstrate storage of charge. The following figure 2 illustrates the device of interest.

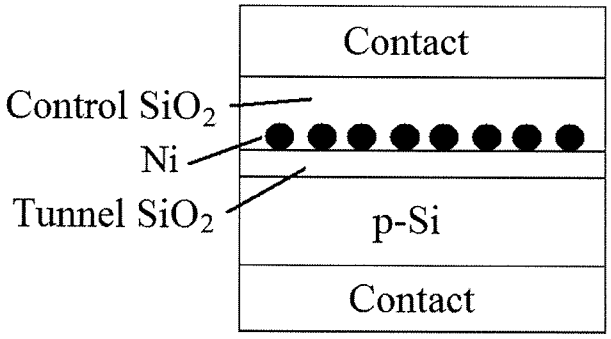

Fig. 2. Ni-ND Device Cross-section

The device illustrated in figure 2 is the basis for this work as it will demonstrate the storage capability of Ni-NDs. The device is a simple MOS capacitor with Ni-NDs in the oxide. The relation of this device to the previously mentioned defects is that Ni-NDs force electrical characteristics similar to that of the defects. The operation of the device is simple in that a positive voltage is applied to the top contact; electrons are attracted from the bulk p-Si into the Ni-NDs structures through Fowler-Nordheim tunneling and are stored. Once charge is stored in the Ni-ND structures the V_{FB} and subsequently the V_T are altered, thus providing different electrical characteristics of the device then when not charged. These characteristics are illustrated by a shift in the high frequency C-V profile of the device and are the result of the V_{FB} shift. This is similar to a shift caused by a fixed oxide charge and can be modeled somewhat similarly. However the shifts in the device are actually engineered and can be controlled with voltages, such as if sufficient enough voltage isn't applied to the gate contact, there will be no V_{FB} shift.

The main advantages of this structure over traditional non-volatile floating gate memory deal with reliability and the decrease in device size. As technology nodes decrease in size, the tunnel oxides must also decrease. This leads to increased probability of failure. One main advantage of the Ni-ND based structure is that a single leakage path in the oxide won't force the device to fail entirely. A typical floating-gate structure has a continuous block of polysilicon instead of Ni-NDs. This element is conductive throughout and if one area begins to leak, all of the charge will leak. With Ni-NDs provided they are electrically isolated, only the Ni-NDs within the vicinity of the weak oxide point will leak; thus allowing improved functionality and reliability. Additionally there exists the potentiality of single memory cells per dot, thus leading to extremely high memory density provided the Ni-NDs are small enough.

III. PROCESS

The fabrication of the Ni-ND structures were performed on p-type silicon. Tunnel oxide was sputtered on using an RF PVD Perkin-Elmer 2400A. Baseline studies were performed on sputtering powers of 200 W, 300 W and 400 W. An operating pressure of 5 mTorr was used with Ar as the sputtering gas. A target of 2 nm was desired for the thickness of the tunnel oxide. It was determined that the tunnel oxide would be sputtered at 200 W for 30 sec with a 5 min pre-sputter of the target. Film thicknesses were measured using a Variable Angle Spectroscopic Ellipsometer (VASE).

Following deposition of the tunnel oxide, a Ni layer with a target of 5 nm was sputtered on the tunnel oxide. Ni was sputtered on using 200 W for 5 sec. The film stack was then measured using the VASE to determine thickness.

Once the Ni was deposited the samples were then thermally annealed in a high temperature anneal furnace to form the Ni-NDs. Temperature treatments of 750°C and 900°C were performed for 10 mins in N_2. Once annealed, the samples were then measured using Atomic Force Microscopy (AFM) to confirm Ni-ND formation and measure surface roughness.

Following Ni-ND formation, the samples were then capped with a control oxide. The control oxide was sputtered on at 200 W for 105 sec. A target of 15 nm was desired for the control oxide thickness. This thickness was measured using the VASE on an untreated control sample which was sputtered with annealed samples.

Once the Ni-ND capacitors were formed, Al contacts were evaporated on the front and back of the samples. A shadow mask was used on the front side of the samples with circular patterns of approximately 0.84 mm diameter.

Devices were then tested electrically using an MDC C-V station to gather the high frequency characteristics of the devices. Sweeps typically ranged from 3 V to -3 V, 2 V to -2 V, 1.5 V to -1.5 V and 1 to -1 V. All sweeps were performed with a retrace.

IV. RESULTS

Ni-NDs were found to have formed at both 750°C and 900°C. The following figure 3 illustrates the initial surface conditions of the Ni pre-anneal.

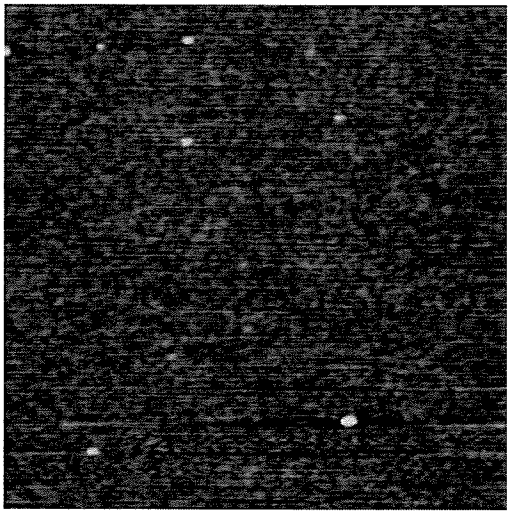

Fig. 3. 1 μm x 1 μm AFM scan of Ni pre-anneal

Once annealed the Ni samples changed morphology drastically, this is illustrated by the comparison of figure 3 and the following figure 4.

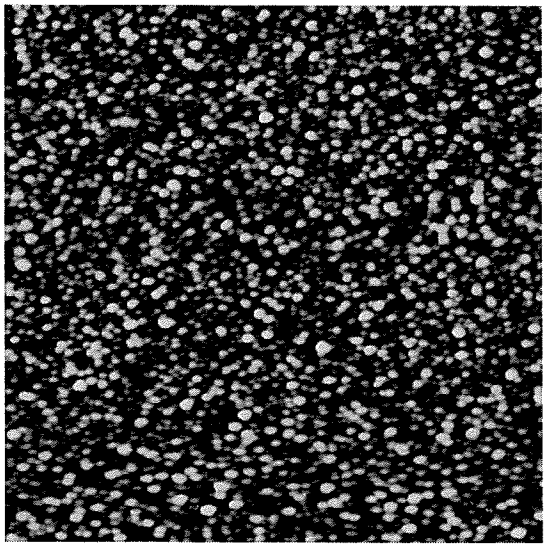

Fig. 4. 2 μm x 2 μm AFM scan of Ni post-anneal at 750°C

The mean roughness of the Ni sample before anneal was found to be 0.141 nm. After anneal the roughness increased to 1.86 nm, thus indicating a formation of nanodots. Ni-ND heights ranged from 3 nm – 15 nm, while their widths ranged from 20 nm – 70 nm and followed a Gaussian distribution in size. The following figure 5 illustrates the roughness data over a range of film thicknesses for the different temperature conditions.

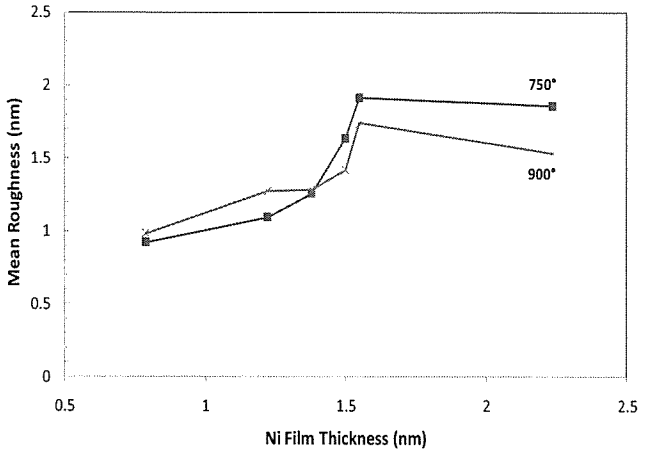

Fig. 5. Ni Film Roughness Post Anneal at 750°C & 900°C

As seen by the above figure 5, there was a general upward trend in film roughness as film thickness increased. Additionally there existed a leveling off effect and a crossing of the two temperature conditions. This possibly indicates a change in the mechanism of their formation as surface diffusion may be playing a larger role as the 750°C samples have a higher roughness.

The electrical measurements performed on the fully structured capacitors yielded fairly positive results. The following figure 6 illustrates the C-V measurements of an oxide only capacitor. This sample was created as a means of comparison with the Ni-ND structures to ensure that the electrical results weren't simply caused by the oxide.

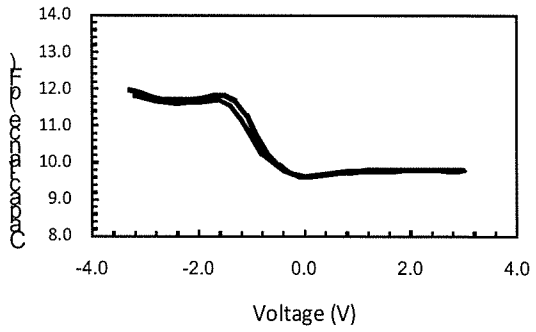

Fig. 6. SiO_2 Capacitor C-V Baseline Results

The oxide only capacitor was found to have only a ΔV_{FB} of -0.02 V. By comparison the Ni-ND structures were found to have a greater shift in V_{FB} which is shown in the following figure 7.

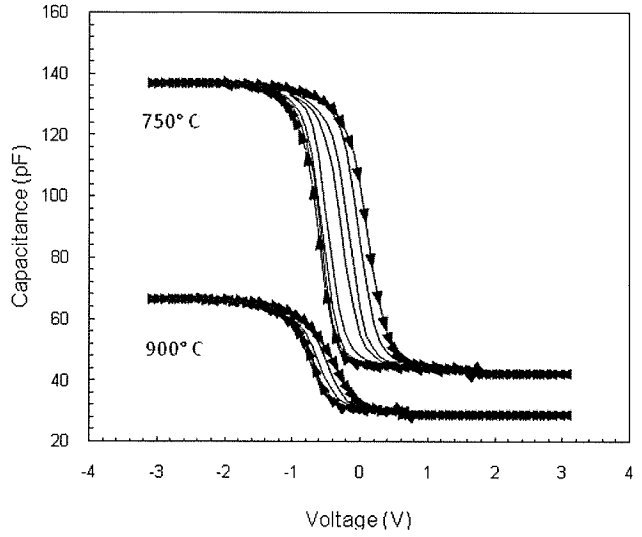

Fig. 7. Ni-ND C-V Test Results of a sample with various treatments

Through the comparison of figures 6 and 7 it can be seen there was a significant shift in the V_{FB} from the Ni-ND structures and the baseline oxide structure. The 750°C annealed device saw a ΔV_{FB} of 0.7 V while the 900°C device saw a 0.1 V shift. The shifts were calculated at a 3 V to -3 V sweep, with the curves shifting positive during the retrace. Additionally it was found that the hysteresis decreased with decreasing voltage range sweeps. This indicated that the hysteresis was somewhat a function of applied voltage. It is believed that the observed hysteresis of the Ni-ND structures is a result of the nanodots storing electrons and forcing the V_{FB} shift. As more negative charge is incorporated in the oxide due to storage, more positive voltage is needed to get the C-V curve to respond.

V. CONCLUSION

Ni-NDs were found to be formed through thermal annealing at temperatures of 750°C and 900°C. A trend of increasing roughness with initial film thickness was also found to exist. Additionally there exhibited a potential change in domination of Ni-ND formation by the mechanisms of evaporation and surface diffusion. This was illustrated through the crossings and leveling off of the mean roughness curves. Future study in terms of roughness and sizing may confirm this. Ni-ND sizes ranged from 3 nm – 15 nm in height and 20 nm – 70 nm in width. While the Ni-NDs formed in this study were found to be tightly bound, they are however too large for integration in future technology nodes. Further optimization could be performed to yield smaller size Ni-NDs. For the applications of this work however, the size of the Ni-NDs was sufficient as relatively large capacitors were fabricated. The electrical characterization from the C-V testing produced fairly positive results as it was believed that the Ni-NDs were storing charge. There exhibited *a ΔV_{FB} of 0.7 V at 750°C and a ΔV_{FB} of 0.1 V at 900°C when swept from 3 V to -3 V. In comparison with the Ni-ND hysteresis, the baseline oxide capacitor only had a ΔV_{FB} of -0.02 V. Additional study on the spacing of the Ni-NDs could be performed in order to determine their electrical isolation characteristics; however as a result of this work it is believed that Ni-NDs have great potential in terms of charge storage and retention.*

ACKNOWLEDGMENT

A.J. Pacifico thanks Dr. Davide Mariotti, Karishma Diwan, Dr. Rommel, Dr. Gupta, Rob Manley, Andrew Estroff, Patrick Whiting for their support during this work. Additionally without the continuous support of the entire SMFL staff at RIT, this work would not be possible.

REFERENCES

[4] R.F. Pierret, *Semiconductor Device Funamentals* .Reading, Ma: Addison-Wesley, 1996, pp. 645–683.

[5] B.V. Zeghbroeck, *Principles of Semiconductor Devices*. Available: http://ece-www.colorado.edu/~bart/book

[6] Yoo-Sung Jang, Jong-Hwan Yoon, and Robert G. Elliman., "Formation of nickel-based nanocrystal monolayers for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 92, pp. 2531-2533, 2008

[7] F.M. Yang, T.C. Change, Po-Tsun Liu, Y.H Yeh, Y.C. Yu, J.Y. Lin, S.M. Sze, and J.C. Lou., "Nickel silicide nanocrystals embedded in SiO2 and HfO2 for nonvolatile memory application," *Thins Solid Films.*, vol. 516, pp. 360-363, 2007

[8] Shang-Chou Chang, Tien-Chia Lin, Jian-Hua Lee, and Kun Shan U., "Converting nickel film to nano particles using hydrogen plasma treatment," *Solid State Technology*, November 2007, pp. 44-46, 2007